CLAIMS

What is claimed is:

1. A high-Q on-chip inductor comprises:

primary winding including a first node and a second node, wherein the primary winding has a first admittance; and

auxiliary winding including a first node and a second node, wherein the auxiliary winding has a second admittance, wherein the second node of the primary winding is coupled to the second node of the auxiliary winding, wherein the second admittance is greater than the first admittance, wherein the first node of the primary winding is operably coupled to receive a first leg of an input, wherein the second node of the primary winding is coupled to receive a second leg of the input, and wherein the first node of the auxiliary winding is coupled to receive a proportionally opposite representation of the first leg of the input.

2. The high-Q on-chip inductor of claim 1, wherein the first admittance includes first self admittance and first coupled admittance and wherein the second admittance includes second self admittance and second coupled admittance.

3. The high-Q on-chip inductor of claim 2, wherein the auxiliary winding is proximally located to the primary winding to at least partially establish the first and second coupled admittances.

4. The high-Q on-chip inductor of claim 2, wherein the auxiliary winding is asymmetric with respect to the primary winding to at least partially establish the second admittance being greater than the first admittance.

5. The high-Q on-chip inductor of claim 4, wherein the asymmetry is achieved by at least one of: asymmetrical electromagnetic coupling between the primary winding and the auxiliary winding, asymmetrical number of turns between the primary winding and the auxiliary winding, and asymmetrical geometric configuration of the primary and auxiliary windings.

6. The high-Q on-chip inductor of claim 1 further comprises a poly-silicon shield operably coupled to the primary winding and to the auxiliary winding.

7. The high-Q on-chip inductor of claim 1 further comprises:

the primary winding including a plurality of turns on multiple dielectric layers of an integrated circuit, wherein the plurality of turns are operably coupled via bridges on differing dielectric layers of the integrated circuit; and

the auxiliary winding including at least one turn on at least one of the multiple dielectric layers of the integrated circuit.

8. The high-Q on-chip inductor of claim 1 further comprises:

the primary winding including at least one turn on a first dielectric layer of an integrated circuit; and

the auxiliary winding including at least one turn on a second dielectric layer of the integrated circuit, wherein the at least one turn of the primary winding is stacked with respect to the at least one turn of the auxiliary winding.

9. A high-Q on-chip inductor comprises:

primary winding including a first node and a second node; and

auxiliary winding operably coupled to increase a quality factor of the primary winding.

10. The high-Q on-chip inductor of claim 9, wherein the auxiliary winding is proximally located to, and reversed biased with respect to, the primary winding to at least partially establish an admittance of the auxiliary winding to be greater than an admittance of the primary winding.

11. The high-Q on-chip inductor of claim 9, wherein the auxiliary winding is asymmetric with respect to the primary winding to at least partially establish an admittance of the auxiliary winding being greater than an admittance of the primary winding.

12. The high-Q on-chip inductor of claim 11, wherein the asymmetry is achieved by at least one of: asymmetrical electromagnetic coupling between the primary winding and the auxiliary winding, asymmetrical number of turns between the primary winding and the auxiliary winding, and asymmetrical geometric configuration of the primary and auxiliary windings.

13. The high-Q on-chip inductor of claim 9 further comprises a poly-silicon shield operably coupled to the primary winding and to the auxiliary winding.

14. The high-Q on-chip inductor of claim 9 further comprises:

the primary winding including a plurality of turns on multiple dielectric layers of an integrated circuit, wherein the plurality of turns are operably coupled via bridges on differing dielectric layers of the integrated circuit; and

the auxiliary winding including at least one turn on at least one of the multiple dielectric layers of the integrated circuit.

15. The high-Q on-chip inductor of claim 9 further comprises:

the primary winding including at least one turn on a first dielectric layer of an integrated circuit; and

the auxiliary winding including at least one turn on a second dielectric layer of the integrated circuit, wherein the at least one turn of the primary winding is stacked with respect to the at least one turn of the auxiliary winding.

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16. A method for manufacturing a high-Q on-chip inductor comprises:

creating a primary winding to include a first node and a second node, wherein the primary winding has a first admittance; and

creating an auxiliary winding to include a first node and a second node, wherein the auxiliary winding has a second admittance, wherein the second node of the primary winding is coupled to the second node of the auxiliary winding, wherein the second admittance is greater than the first admittance, wherein the first node of the primary winding is operably coupled to receive a first leg of an input, wherein the second node of the primary winding is coupled to receive a second leg of the input, and wherein the first node of the auxiliary winding is coupled to receive a proportionally opposite representation of the first leg of the input.

17. The method of claim 16 further comprises:

creating the primary winding to have the first admittance that includes first self admittance and first coupled admittance; and

creating the auxiliary winding to have the second admittance that includes second self admittance and second coupled admittance.

18. The method of claim 17 further comprises:

creating the auxiliary winding to be proximally located to the primary winding such that at least part of the first and second coupled admittances are established.

19. The method of claim 17 further comprises:

creating the auxiliary winding to be asymmetric with respect to the primary winding such that the second admittance is greater than the first admittance.

20. The method of claim 19 further comprises creating the asymmetry by at least one of:

asymmetrical electromagnetic coupling the primary winding to the auxiliary winding;

creating number of turns of the primary winding to be different than a number of turns of the auxiliary winding; and

creating the primary winding to have different geometric configuration than the auxiliary winding.

21. The method of claim 16 further comprises:

creating a poly-silicon shield that is operably coupled to the primary winding and to the auxiliary winding.

22. The method of claim 16 further comprises:

creating the primary winding to include a plurality of turns on multiple dielectric layers of an integrated circuit,

coupling the plurality of turns via bridges on differing dielectric layers of the integrated circuit; and

creating the auxiliary winding including at least one turn on at least one of the multiple dielectric layers of the integrated circuit.

23. The method of claim 16 further comprises:

creating the primary winding to include at least one turn on a first dielectric layer of an integrated circuit; and

creating the auxiliary winding to include at least one turn on a second dielectric layer of the integrated circuit in a stacked configuration with respect to the at least one turn of the primary winding.

24. A method for manufacturing a high-Q on-chip inductor comprises:

creating a primary winding to include a first node and a second node; and

creating an auxiliary winding operably coupled to increase a quality factor of the primary winding.

25. The method of claim 24 further comprises:

creating the auxiliary winding to be proximally located to, and reversed biased with respect to, the primary winding such that an admittance of the auxiliary winding is greater than an admittance of the primary winding.

26. The method of claim 24 further comprises:

creating the auxiliary winding to be asymmetric with respect to the primary winding to at least partially establish an admittance of the auxiliary winding being greater than an admittance of the primary winding.

27. The method of claim 26 further comprises creating the asymmetry by at least one of:

asymmetrical electromagnetic coupling the primary winding to the auxiliary winding;

creating the primary winding to have a differing number of turns than a number of turns of the auxiliary winding; and

creating the primary winding to have an asymmetrical geometric configuration with respect to the auxiliary winding.

28. The method of claim 24 further comprises:

creating a poly-silicon shield operably coupled to the primary winding and to the auxiliary winding.

29. The method of claim 24 further comprises:

creating the primary winding to include a plurality of turns on multiple dielectric layers of an integrated circuit;

connecting the plurality of turns of the primary winding using bridges on differing dielectric layers of the integrated circuit; and

creating the auxiliary winding to include at least one turn on at least one of the multiple dielectric layers of the integrated circuit.

30. The method of claim 24 further comprises:

creating the primary winding to include at least one turn on a first dielectric layer of an integrated circuit; and

creating the auxiliary winding to include at least one turn on a second dielectric layer of the integrated circuit in a stacked configuration with respect to the at least one turn of the primary winding.